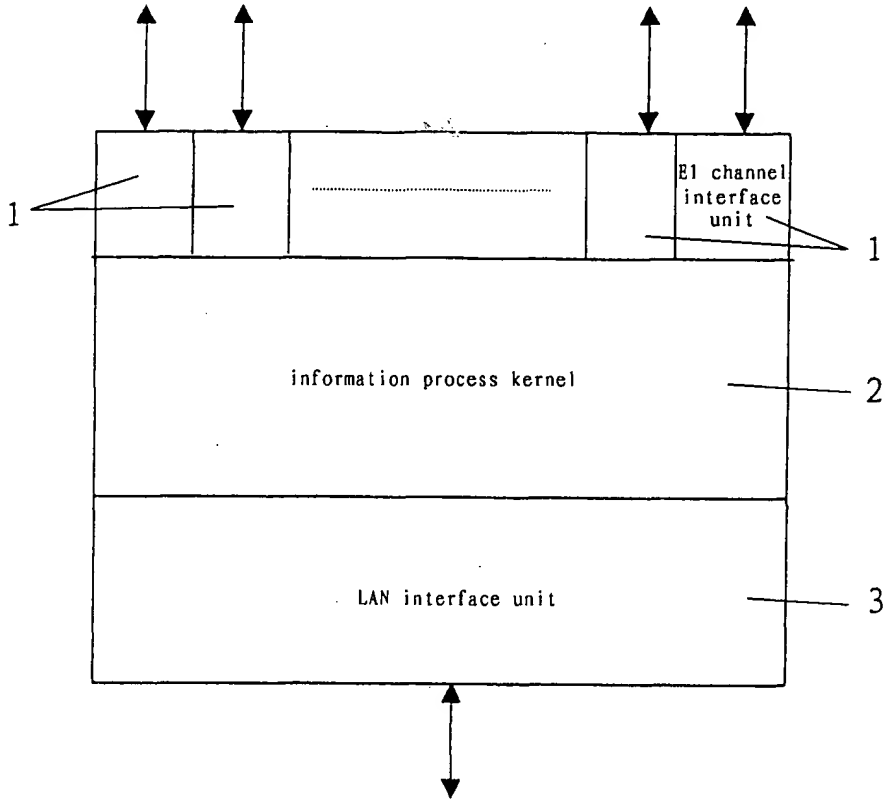

E1 channel interface unit
1
1
information process kernel
2
LAN interface unit
3

Fig. 1

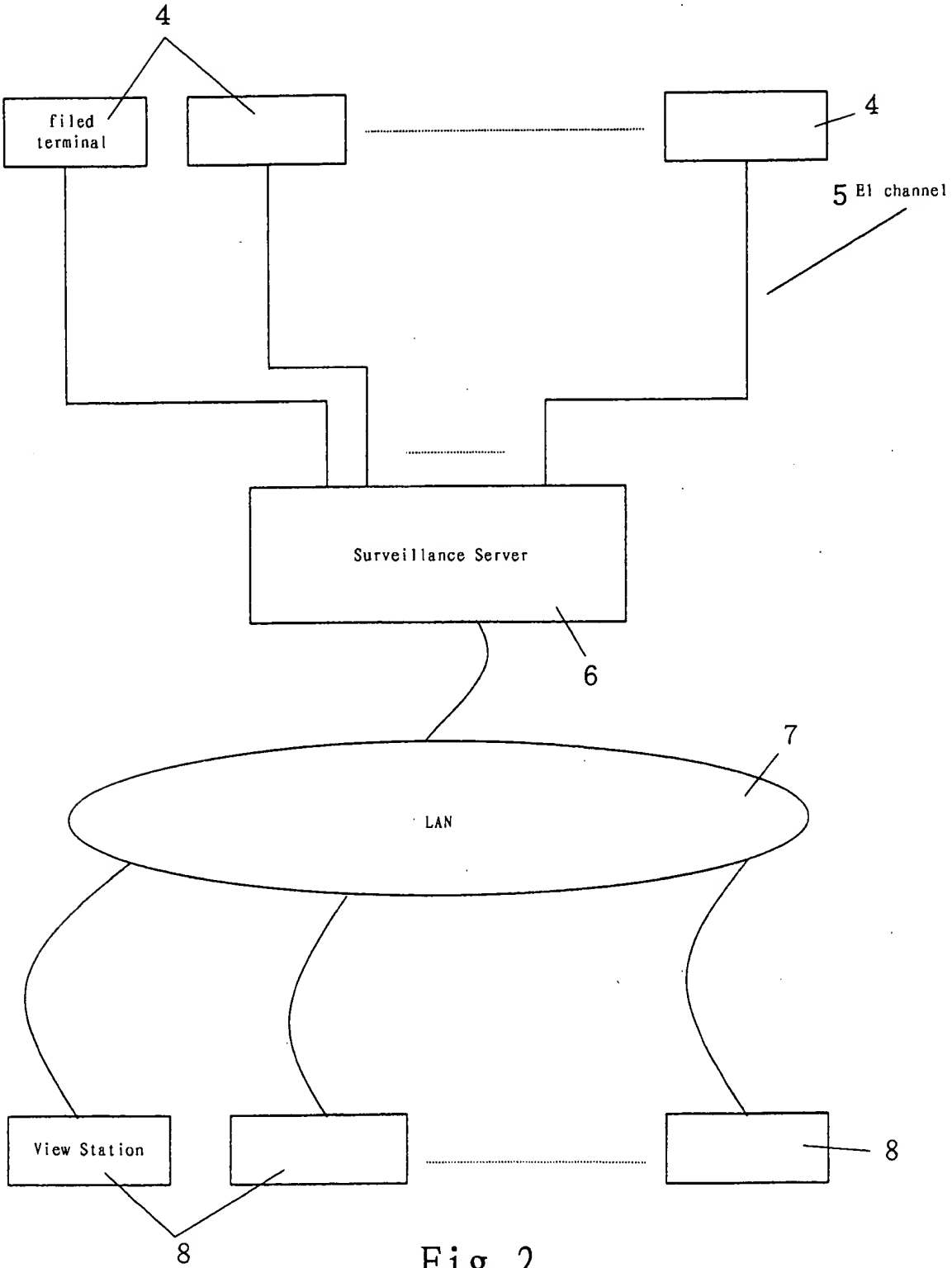

4
filed terminal
4
5 E1 channel
Surveillance Server
6
7
LAN
View Station
8
8

Fig. 2

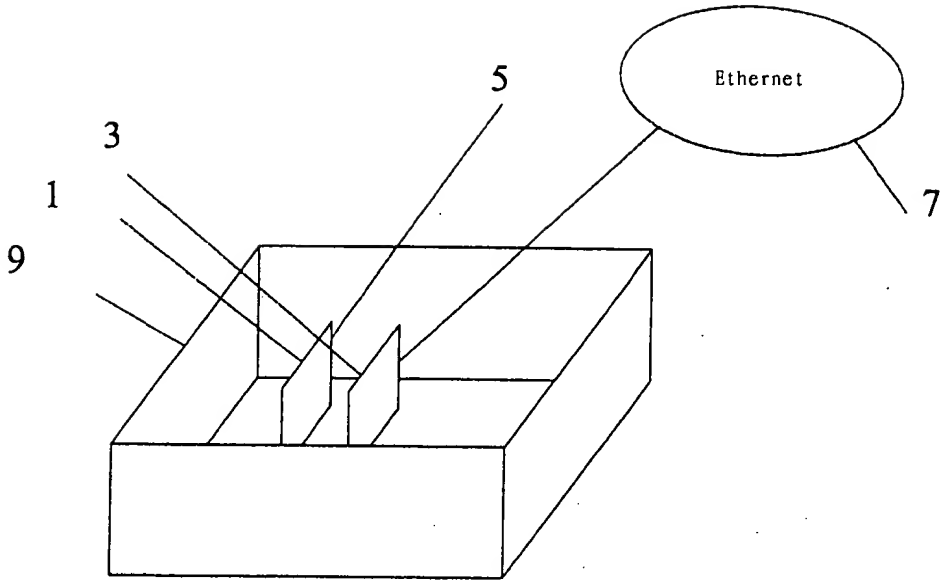


Fig. 3

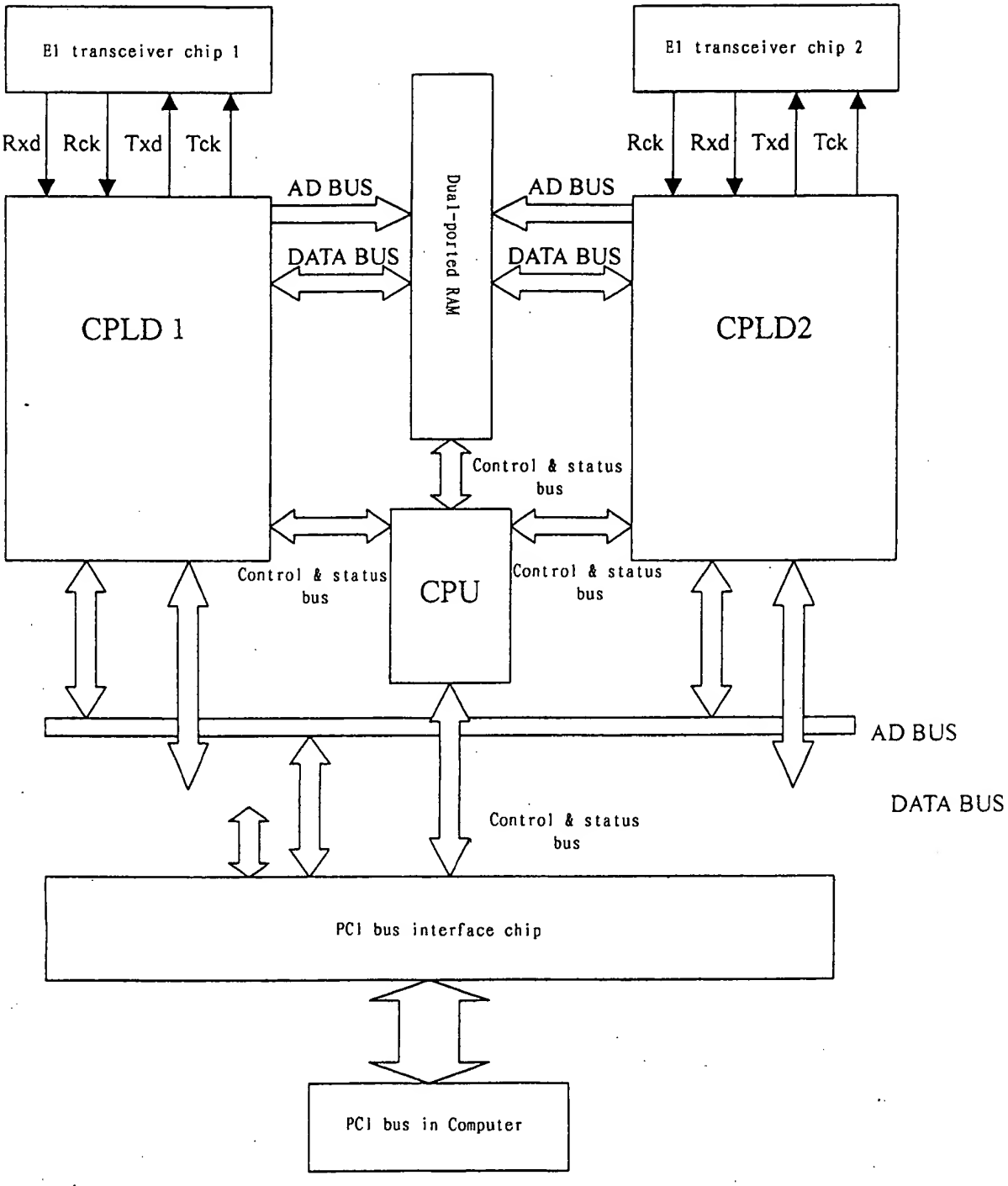

E1 transceiver chip 1
E1 transceiver chip 2
Rxd
Rck
Txd
Tck
Rck
Rxd
Txd
Tck
AD BUS
AD BUS
Dual-ported RAM
DATA BUS
DATA BUS
CPLD 1
CPLD2
Control & status bus
Control & status bus
CPU
Control & status bus
AD BUS
DATA BUS
Control & status bus
PCI bus interface chip
PCI bus in Computer

Fig. 4

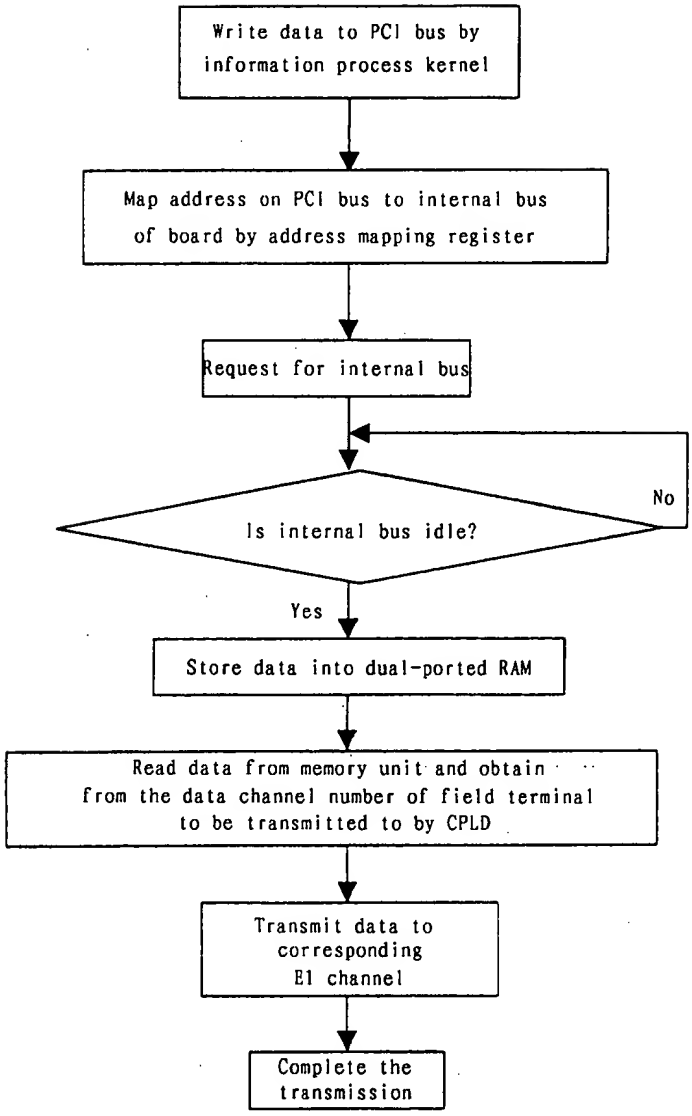

Write data to PCI bus by information process kernel
Map address on PCI bus to internal bus of board by address mapping register
Request for internal bus
Is internal bus idle?
No
Yes
Store data into dual-ported RAM
Read data from memory unit and obtain from the data channel number of field terminal to be transmitted to by CPLD
Transmit data to corresponding E1 channel
Complete the transmission

Fig. 5

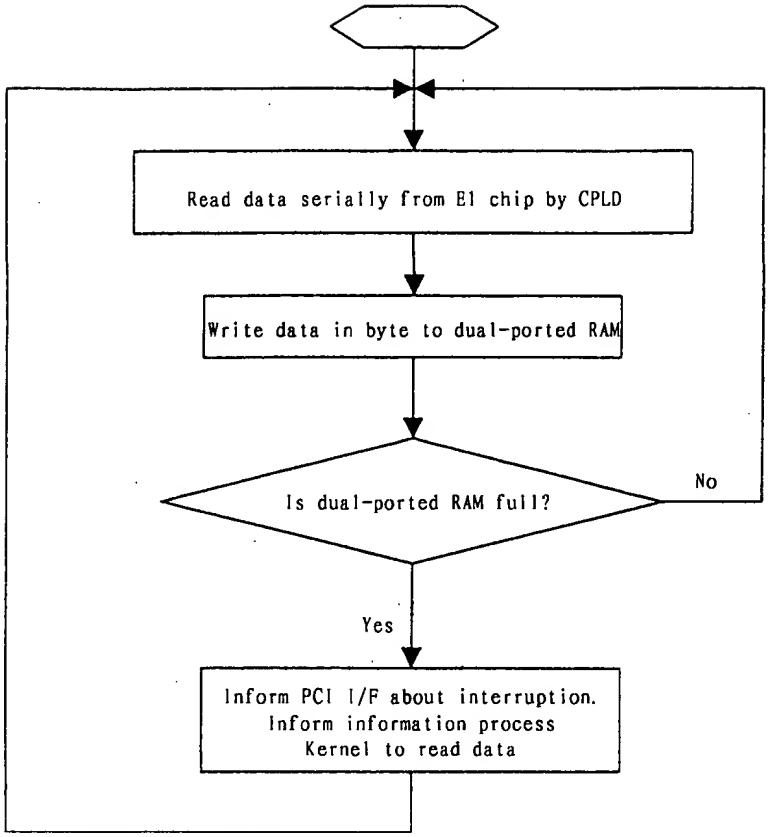

Read data serially from E1 chip by CPLD
Write data in byte to dual-ported RAM
Is dual-ported RAM full?
No
Yes
Inform PCI I/F about interruption.
Inform information process
Kernel to read data

Fig. 6

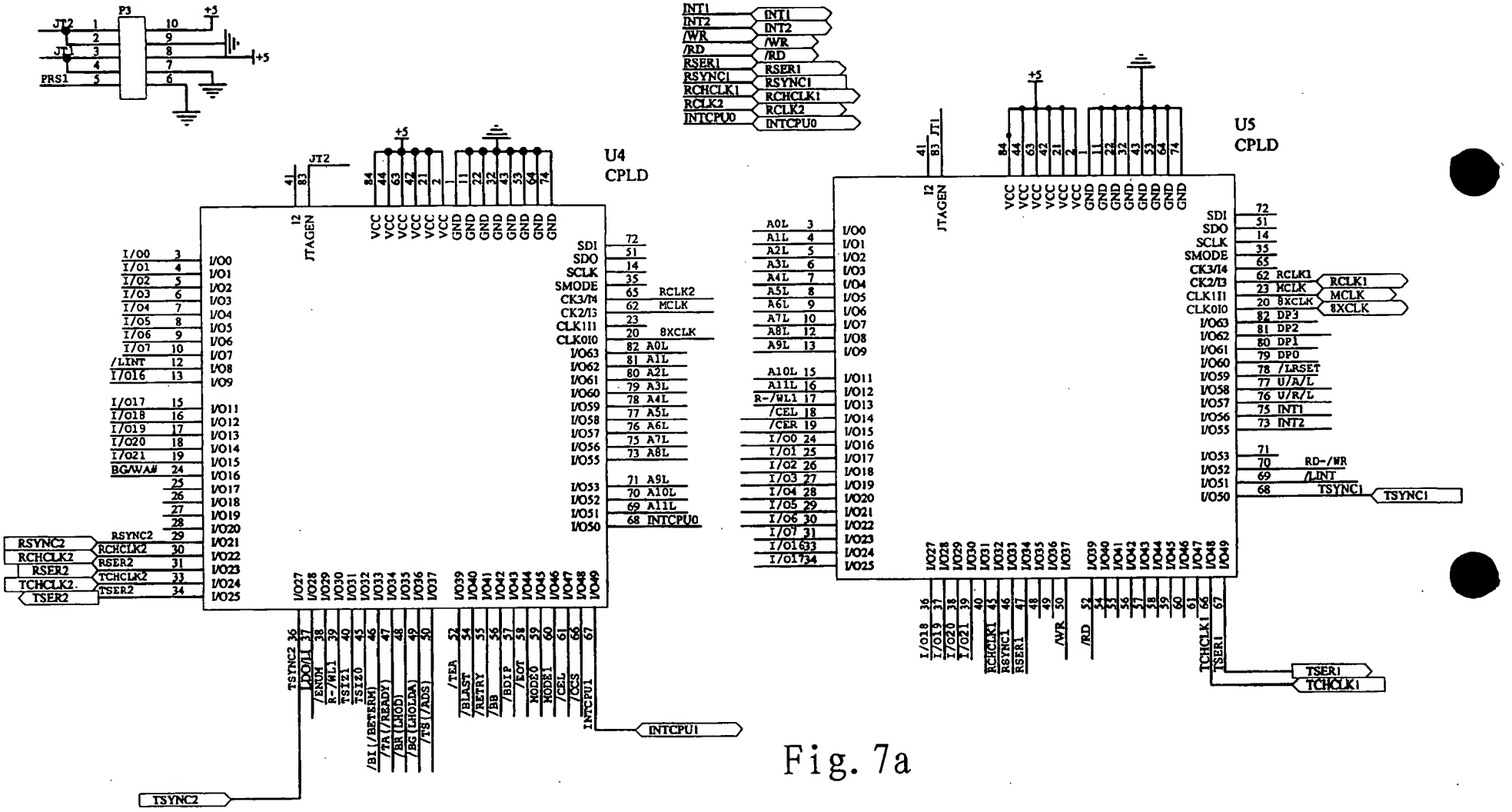


Fig. 7a

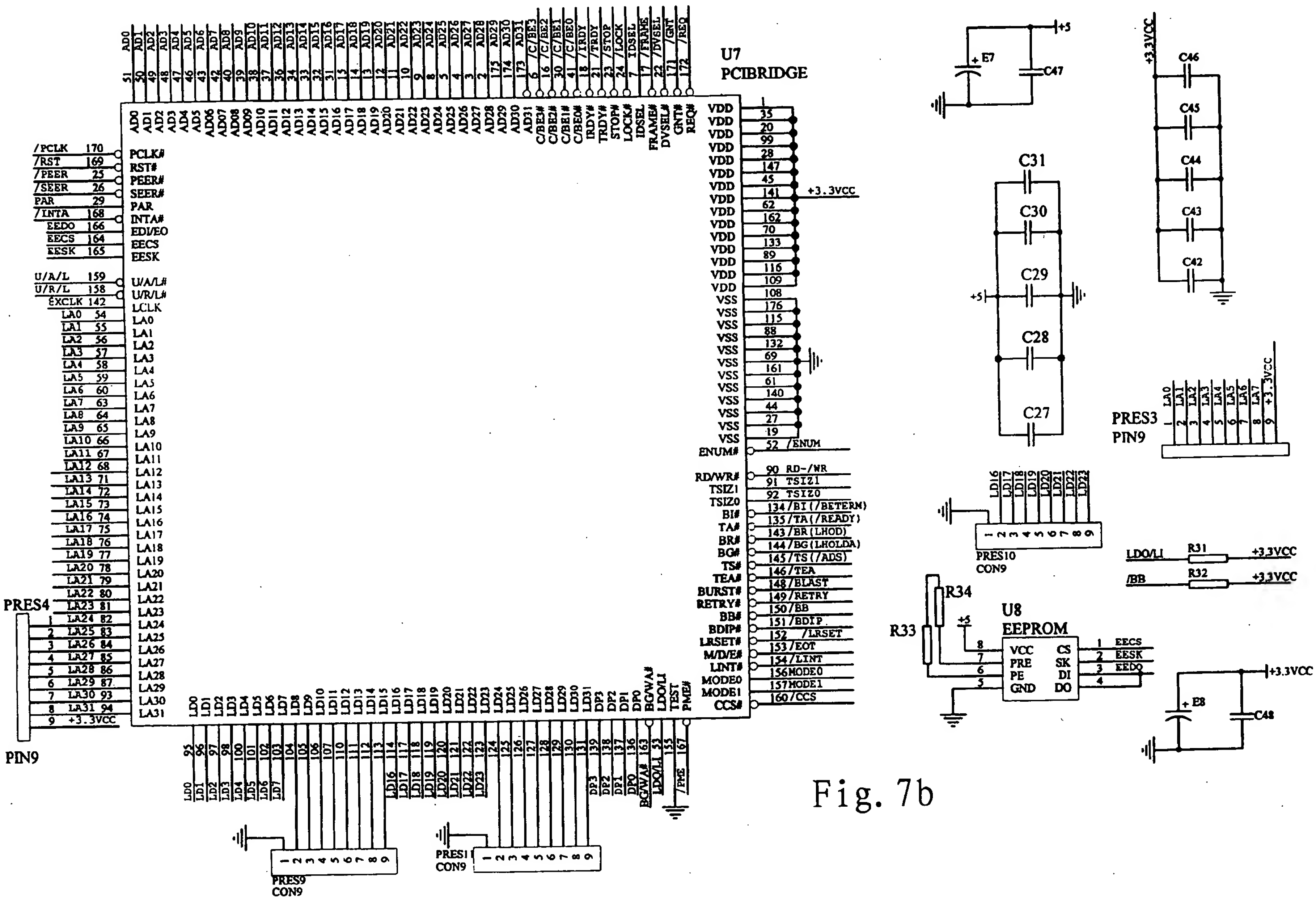
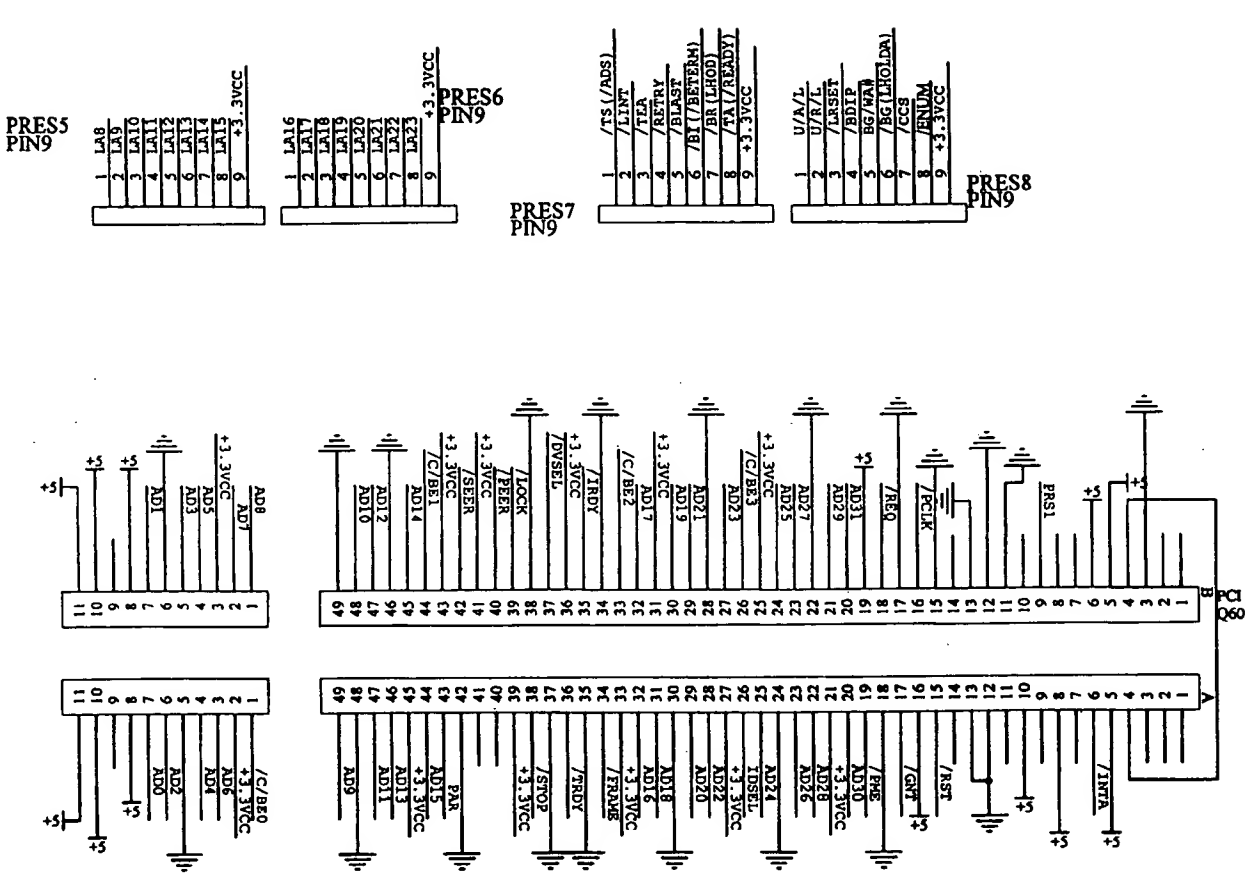

U7
PCIBRIDGE
U8
EEPROM
PRES3
PIN9
PRES4
PIN9
PRES9
CON9
PRES10
CON9
PRES11
CON9
E7
C47
E8
C48
C27
C28
C29
C30
C31
C42
C43
C44
C45
C46
R31
R32
R33
R34
+3.3VCC
+5

Fig. 7b


PRES5
PIN9
PRES6
PIN9
PRES7
PIN9
PRES8
PIN9
PCI
Q60

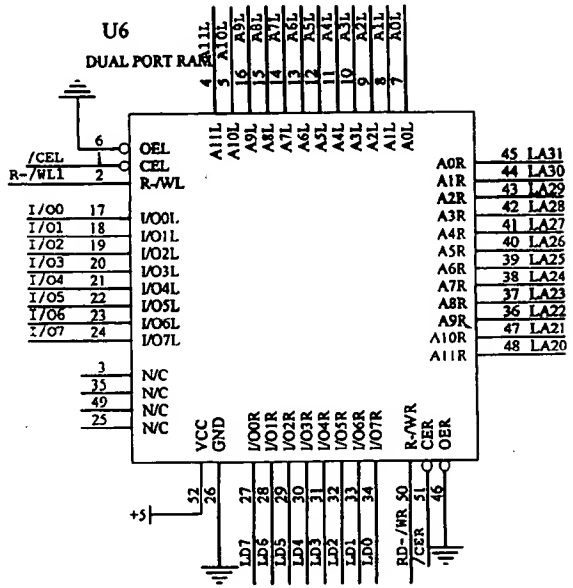

U6
DUAL PORT RAM

Fig. 7c

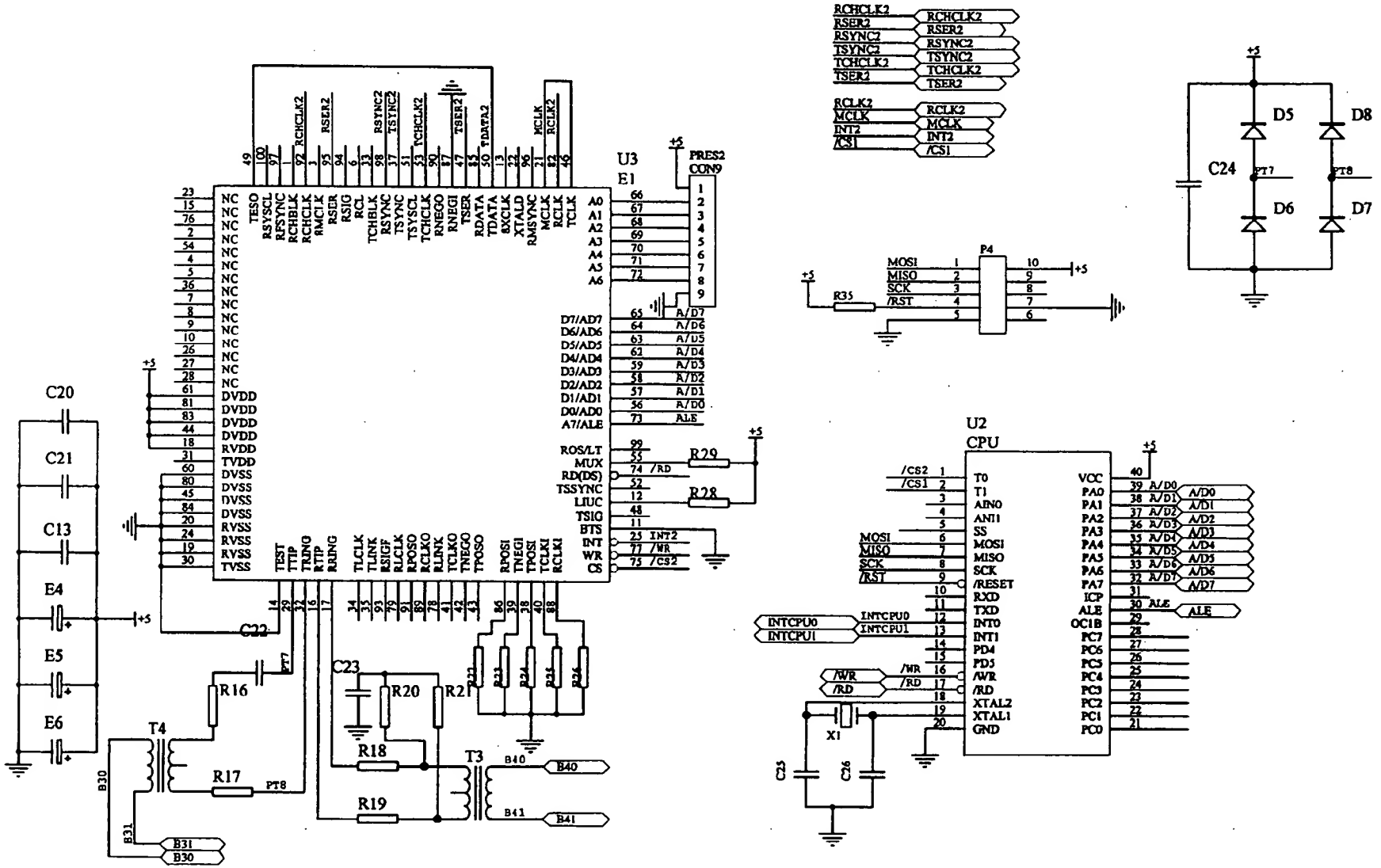


Fig. 8

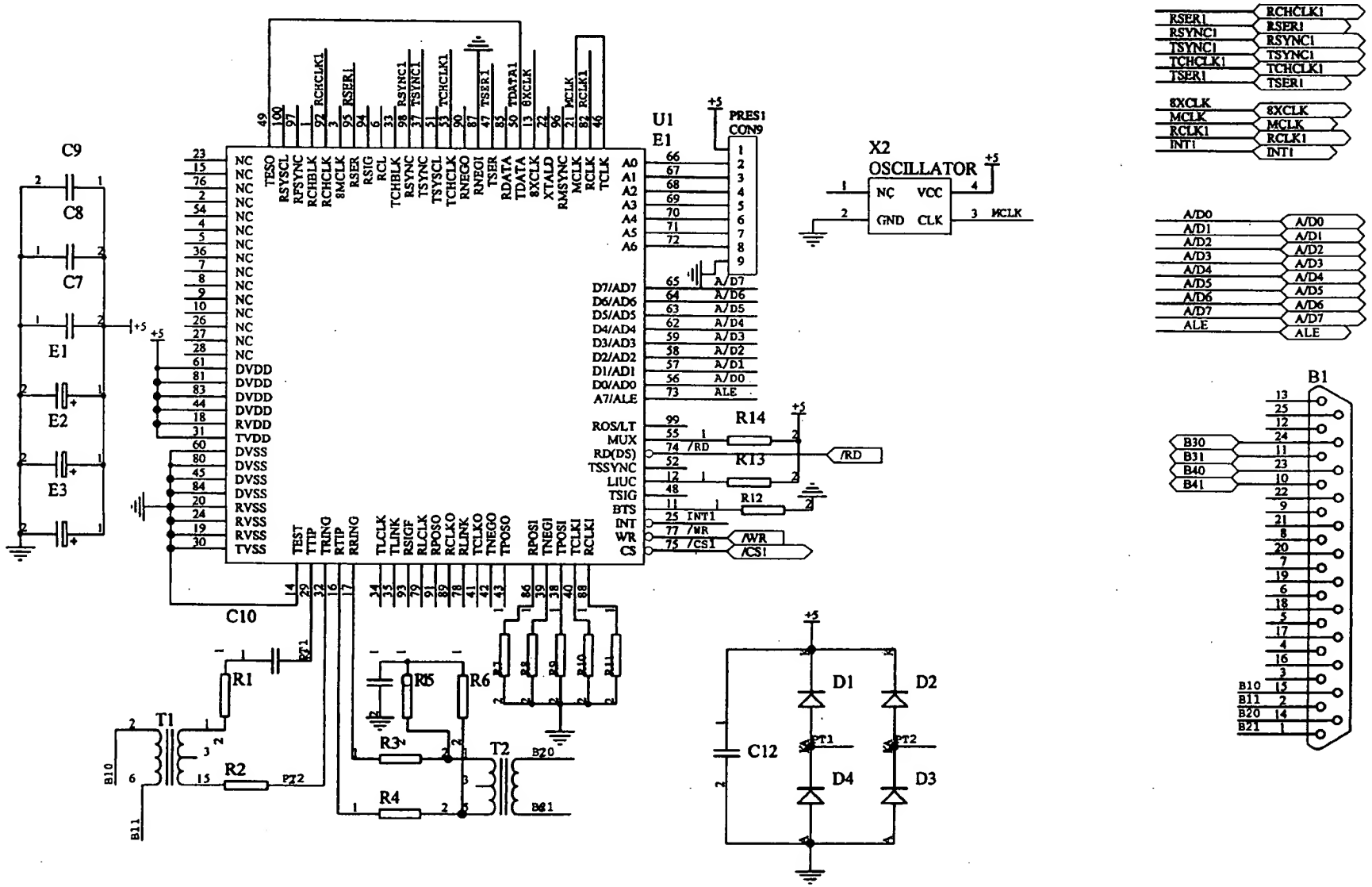


Fig. 9